

FIG. 2 (PRIOR ART)

are defective, but a product is processed as nondefective

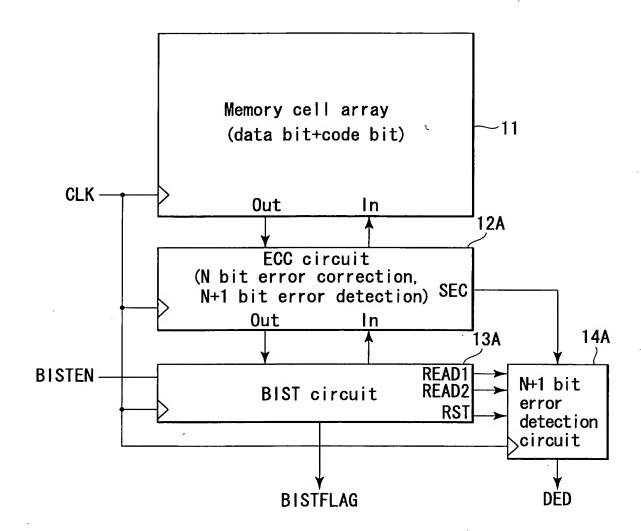
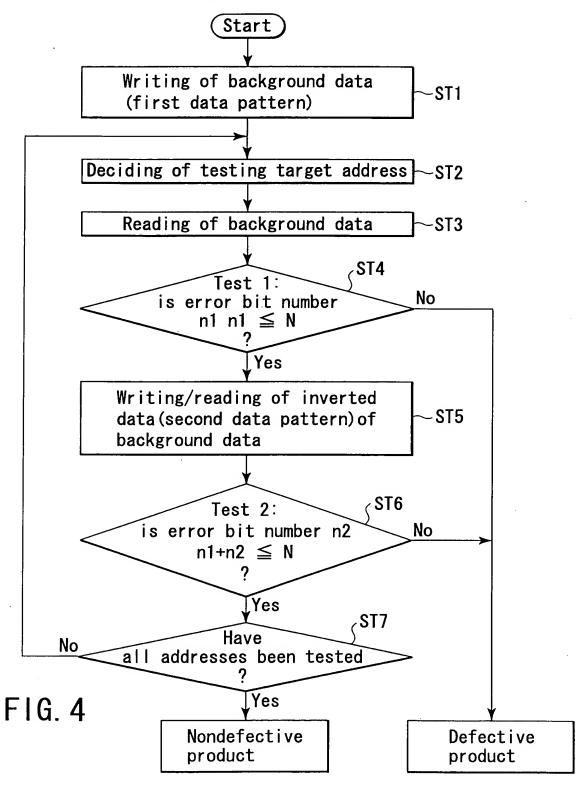


FIG. 3

Test method 1 (in the case of memory on which ECC circuit capable of N bit error correction, N+1 bit error detection is mounted)



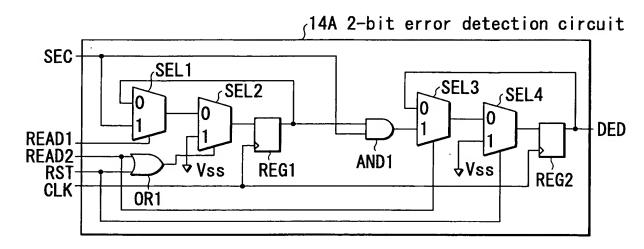
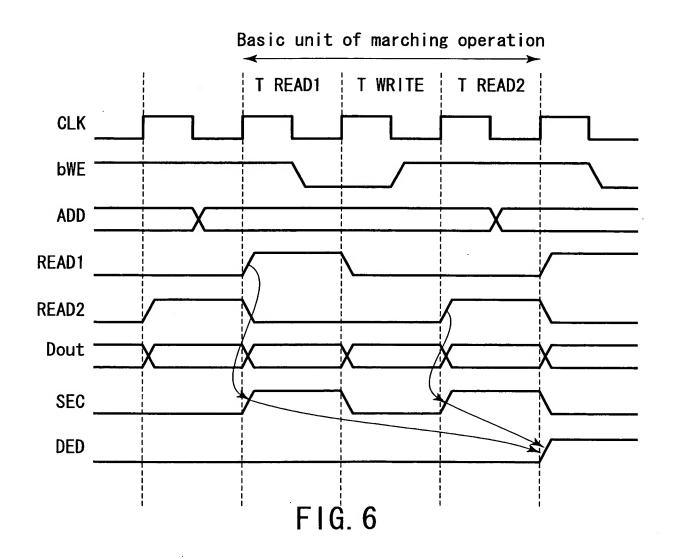


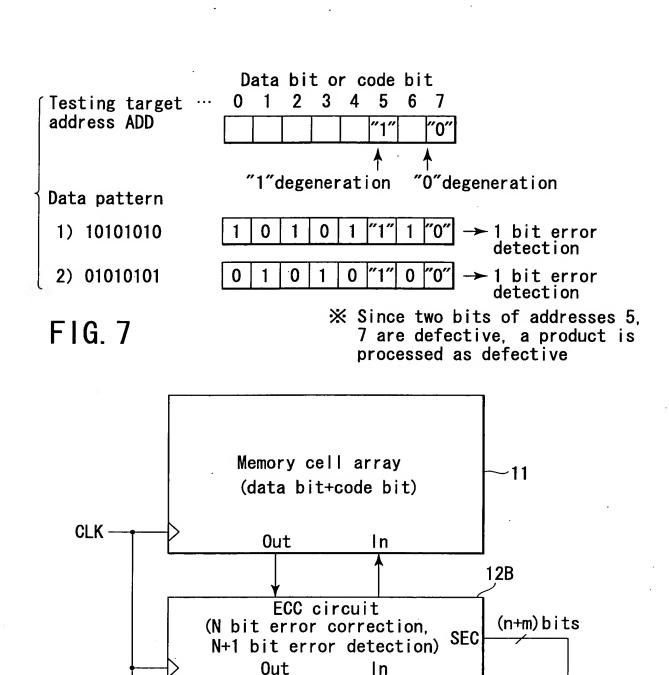
FIG. 5



3 4 1 3

**BISTEN-**

FIG. 8



BIST circuit

BISTFLAG

13B

N+1 bit

detection circuit

DED

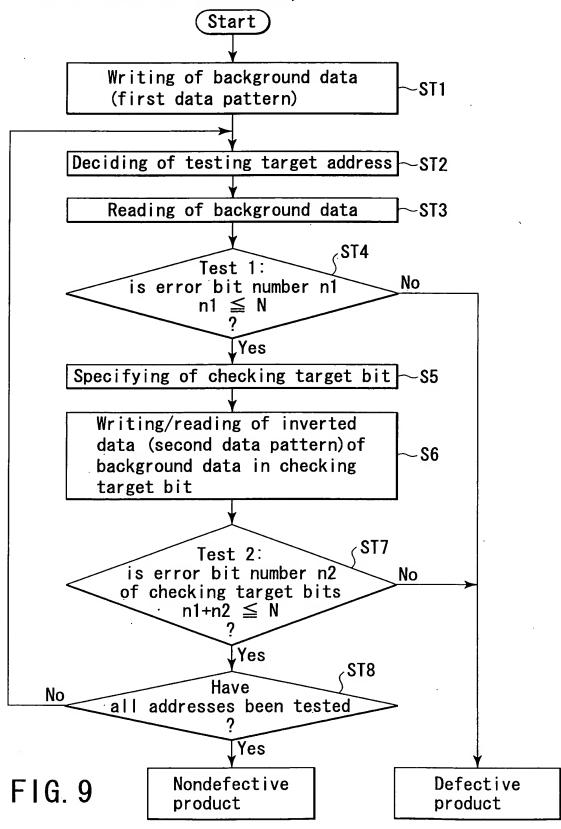
error

STATE

READ1

READ2

Test method 2(in the case of memory on which ECC circuit capable of N bit error correction, N+1 bit error detection is mounted)



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Data bit (n bit)

Code bit (m bit)

0 1 2 3 4 5 6 7 Testing target ... a b c d e address Data pattern 1) 10101010 2) 01010101 0 Checking target bit Checking target bit X In test 2, addresses a, FIG. 10 b, e are not checked Data bit (n bit) Testing target ... address Data pattern FIG. 11 1) 1010\*\*\*\* 0 2) 0101\*\*\*\* Checking target bit **※** Addresses 4, 5, 6, 7 are not tested

